



8 x 8 Video Crosspoint Switch

MAX456

General Description

The MAX456 is the first monolithic CMOS 8 x 8 video crosspoint switch that significantly reduces component count, board space, and cost. The crosspoint switch contains a digitally controlled matrix of 64 T-switches that connect eight video input signals to any, or all, output channels. Each matrix output connects to eight internal, high-speed (250V/μs), unity-gain-stable buffers capable of driving 400Ω and 20pF to ±1.3V. For applications requiring increased drive capability, the MAX456 outputs can be connected directly to two MAX470 quad, gain-of-two video buffers, which are capable of driving 75Ω loads.

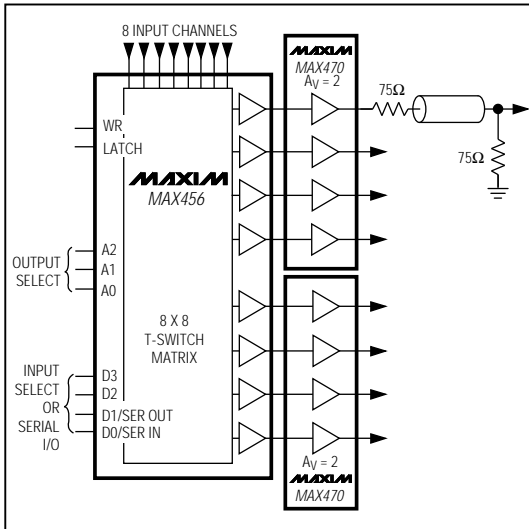
Three-state output capability and internal, programmable active loads make it feasible to parallel multiple MAX456s and form larger switch matrices.

In the 40-pin DIP package, crosstalk (70dB at 5MHz) is minimized, and board area and complexity are simplified by using a straight-through pinout. The analog inputs and outputs are on opposite sides, and each channel is separated by a power-supply line or quiet digital logic line.

Applications

- Video Test Equipment
- Video Security Systems
- Video Editing

Typical Application Circuit



Features

- ◆ Routes Any Input Channel to Any Output Channel
- ◆ Switches Standard Video Signals
- ◆ Serial or Parallel Digital Interface
- ◆ Expandable for Larger Switch Matrices
- ◆ 80dB All-Channel Off Isolation at 5MHz
- ◆ 8 Internal Buffers with:
 - 250V/μs Slew Rate, Three-State Output Capability, Power-Saving Disable Feature, 35MHz Bandwidth

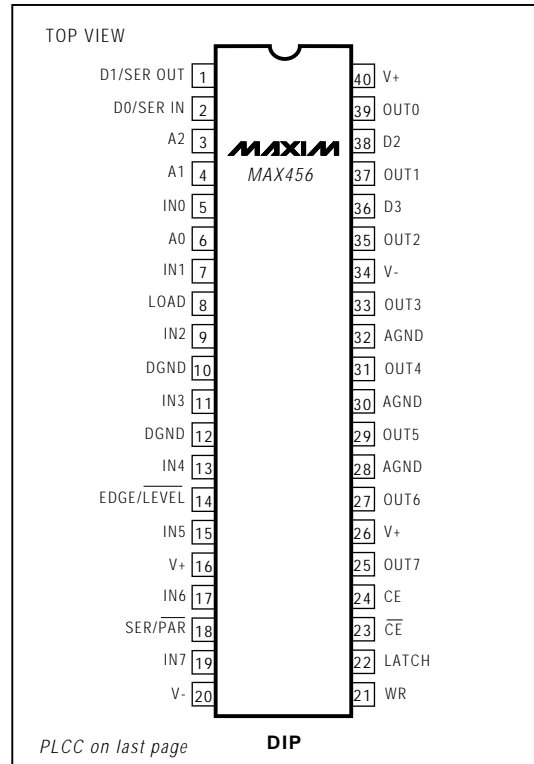
Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|-----------|--------------|----------------|
| MAX456CPL | 0°C to +70°C | 40 Plastic DIP |
| MAX456CQH | 0°C to +70°C | 44 PLCC |
| MAX456C/D | 0°C to +70°C | Dice* |

Ordering Information continued on last page.

* Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

Pin Configurations



PLCC on last page



8 x 8 Video Crosspoint Switch

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-)+12V
 Positive Supply Voltage V+ Referred to AGND-0.3V to +12V
 Negative Supply Voltage V- Referred to AGND-12V to +0.3V
 DGND VoltageAGND $\pm 0.3V$
 Buffer Short Circuit to Ground when
 Not Exceeding Package Power DissipationIndefinite
 Analog Input Voltage(V+ + 0.3V) to (V- - 0.3V)
 Digital Input Voltage(V+ + 0.3V) to (V- - 0.3V)
 Input Current, Power On or Off
 Digital Inputs $\pm 20mA$
 Analog Inputs $\pm 50mA$

Continuous Power Dissipation ($T_A = +70^\circ C$)
 40-Pin Plastic DIP (derate 11.3mW/ $^\circ C$ above +70 $^\circ C$)889mW
 40-Pin CERDIP (derate 20.0mW/ $^\circ C$ above +70 $^\circ C$)1600mW
 44-Pin PLCC (derate 13.3mW/ $^\circ C$ above +70 $^\circ C$)1066mW
 Operating Temperature Ranges:
 MAX456C _ _0 $^\circ C$ to +70 $^\circ C$
 MAX456E _ _-40 $^\circ C$ to +85 $^\circ C$
 Storage Temperature Range-65 $^\circ C$ to +160 $^\circ C$
 Lead Temperature (soldering, 10 sec)+300 $^\circ C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5.0V, V- = -5.0V, -1.3V $\leq V_{IN} \leq$ +1.3V; LOAD = +5V; internal load resistors on; AGND = DGND = 0V; $T_A = +25^\circ C$, unless otherwise noted.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|--|------------------------------|-----------|-----|-----------|-----------|
| Input Voltage Range | | | -1.3 | | 1.3 | V |
| Voltage Gain | Internal load resistors on, no external load, $V_{IN} = 0V$ to 1V | $T_A = +25^\circ C$ | 0.99 | 1.0 | 1.01 | V/V |
| | | $T_A = T_{MIN}$ to T_{MAX} | 0.98 | 1.0 | 1.02 | |
| Buffer Offset Voltage | $T_A = +25^\circ C$ | | | | | ± 7 |
| | $T_A = T_{MIN}$ to T_{MAX} | | | | | ± 12 |
| Offset Voltage Drift | $T_A = T_{MIN}$ to T_{MAX} | | | | | 20 |
| Operating Supply Voltage | | | ± 4.5 | | ± 5.5 | V |
| Supply Current, All Buffers On (No External Load) | $T_A = +25^\circ C$ | | | | | 39 |
| | $T_A = T_{MIN}$ to T_{MAX} | | | | | 45 |
| Supply Current, All Buffers Off | $T_A = +25^\circ C$ | | | | | 1.5 |
| | $T_A = T_{MIN}$ to T_{MAX} | | | | | 3.0 |
| Power-Supply Rejection Ratio | $\pm 4.5V$ to $\pm 5.5V$, DC measurement | | 50 | 64 | | dB |
| Analog Input Current | $T_A = T_{MIN}$ to T_{MAX} | | | | | ± 0.1 |
| Output Leakage Current | Internal load resistors off, all buffers off, $T_A = T_{MIN}$ to T_{MAX} | | | | | ± 100 |
| Internal Amplifier Load Resistor (LOAD Pin = 5V) | $T_A = +25^\circ C$ | | 250 | 400 | 600 | Ω |
| | $T_A = T_{MIN}$ to T_{MAX} | | 200 | | 765 | |
| Buffer Output Voltage Swing | Internal load resistors on, no external load | | | | | ± 1.3 |
| Digital Input Current | $T_A = T_{MIN}$ to T_{MAX} | | | | | ± 1 |
| Output Impedance at DC | | | | | | 10 |
| Input Logic Low Threshold | | | | | | 0.8 |
| Input Logic High Threshold | | | | | | 2.4 |
| SER OUT Output Logic Low | Serial mode, SER/PAR = 5V | $I_{OL} = 1.6mA$ | | | | 0.4 |
| SER OUT Output Logic High | | $I_{OH} = -0.4mA$ | | | | 4 |

8 x 8 Video Crosspoint Switch

MAX456

ELECTRICAL CHARACTERISTICS

($V_+ = 5.0V$, $V_- = -5.0V$, $-1.3V \leq V_{IN} \leq +1.3V$, $LOAD = +5V$, internal load resistors on, $AGND = DGND = 0V$, $T_A = +25^\circ C$, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--|-----|-----|-----|-------------------|
| DYNAMIC SPECIFICATIONS (Note 1) | | | | | |
| Output-Buffer Slew Rate | Internal load resistors on, 10pF load | | 250 | | V/ μ s |
| Single-Channel Crosstalk | 5MHz, $V_{IN} = 2V_{P-P}$ (Note 2) | 60 | 70 | | dB |
| All-Channel Crosstalk | 5MHz, $V_{IN} = 2V_{P-P}$ (Notes 2, 3) | | 57 | | dB |
| All-Channel Off Isolation | 5MHz, $V_{IN} = 2V_{P-P}$ (Note 2) | | 80 | | dB |
| -3dB Bandwidth | 10pF load, $V_{IN} = 2V_{P-P}$ (Note 2) | 25 | 35 | | MHz |
| Differential Phase Error | (Note 4) | | 1.0 | | deg |
| Differential Gain Error | (Note 4) | | 0.5 | | % |
| Input Noise | DC to 40MHz | | 0.3 | 1.0 | mV _{RMS} |
| Input Capacitance | All buffer inputs grounded | | 6 | | pF |
| Buffer Input Capacitance | Additional capacitance for each output buffer connected to channel input | | 2 | | pF |
| Output Capacitance | Output buffer off | | 7 | | pF |

SWITCHING CHARACTERISTICS (Note 1)

(Figure 4, $V_+ = 5.0V$, $V_- = -5.0V$, $-1.3V \leq V_{IN} \leq +1.3V$, $LOAD = +5V$, internal load resistors on, $AGND = DGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--------------------------------|--------------------|--------------------|-----|-----|-----|-------|
| Chip-Enable to Write Setup | t_{CE} | | 0 | | | ns |
| Write Pulse Width High | t_{WH} | | 80 | | | ns |
| Write Pulse Width Low | t_{WL} | | 80 | | | ns |
| Data Setup | t_{DS} | Parallel mode | 240 | | | ns |
| | | 32-bit serial mode | 160 | | | |
| Data Hold | t_{DH} | | 0 | | | ns |
| Latch Pulse Width | t_L | | 80 | | | ns |
| Latch Delay | t_D | | 80 | | | ns |
| Switch Break-Before-Make Delay | $t_{ON} - t_{OFF}$ | | | 15 | | ns |
| LATCH Edge to Switch Off | t_{OFF} | LATCH on | | 35 | | ns |
| LATCH Edge to Switch On | t_{ON} | | | 50 | | ns |

Note 1: Guaranteed by design.

Note 2: See *Dynamic Test Circuits* on page 11.

Note 3: 3dB typical crosstalk improvement when $R_S = 0\Omega$.

Note 4: Input test signal: 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0 to 100IRE). IRE is a unit of video-signal amplitude developed by the International Radio Engineers. 140IRE = 1.0V.

8 x 8 Video Crosspoint Switch

Pin Description

| PIN | | NAME | FUNCTION |
|--------------------------------|--------------------------------|---------------------------------|---|
| DIP | PLCC | | |
| — | 1, 12, 23, 34 | N.C. | No connect. Not internally connected. |
| 1 | 2 | D1/SER OUT | Parallel Data Bit D1 when SER/ $\overline{\text{PAR}}$ = 0V. Serial Output for cascading multiple parts when SER/ $\overline{\text{PAR}}$ = 5V. |
| 2 | 3 | D0/SER IN | Parallel Data Bit D0 when SER/ $\overline{\text{PAR}}$ = 0V. A Serial Input when SER/ $\overline{\text{PAR}}$ = 5V. |
| 3, 4, 6 | 4, 5, 7 | A2, A1, A0 | Output Buffer Address Lines |
| 5, 7, 9, 11, 13, 15, 17, 19 | 6, 8, 10, 13, 15, 17, 19, 21 | IN0-IN7 | Video Input Lines |
| 8 | 9 | LOAD | Asynchronous control line. When LOAD = 1, all the 400 Ω internal active loads are on. When LOAD = 0, external 400 Ω loads must be used. The buffers MUST have a resistive load to maintain stability. |
| 10, 12 | 11, 14 | DGND | Digital Ground Pins. Both DGND pins must have the same potential and be bypassed to AGND. DGND should be within $\pm 0.3V$ of AGND. |
| 14 | 16 | EDGE/ $\overline{\text{LEVEL}}$ | When this control line is high, the 2nd-rank registers are loaded with the rising edge of the LATCH line. If this control line is low, the 2nd-rank registers are transparent when LATCH is low, passing data directly from the 1st-rank registers to the decoders. |
| 16, 26, 40 | 18, 29, 44 | V+ | All V+ pins must be tied to each other and bypassed to AGND separately (Figure 2). |
| 18 | 20 | SER/ $\overline{\text{PAR}}$ | 5V = 32-Bit Serial, 0V = 7-Bit Parallel |
| 20, 34 | 22, 38 | V- | Both V- pins must be tied to each other and bypassed to AGND separately (Figure 2). |
| 21 | 24 | WR | WRITE in the serial mode, shifts data in. In the parallel mode, WR loads data into the 1st-rank registers. Data is latched on the rising edge. |
| 22 | 25 | LATCH | If EDGE/ $\overline{\text{LEVEL}}$ = 5V, data is loaded from the 1st-rank registers to the 2nd-rank registers on the rising edge of LATCH. If EDGE/ $\overline{\text{LEVEL}}$ = 0V, data is loaded while LATCH = 0V. In addition, data is loaded during the execution of parallel-mode functions 1011 through 1110, or if LATCH = 5V during the execution of the parallel-mode "software-LATCH" command (1111). |
| 23 | 26 | $\overline{\text{CE}}$ | Chip Enable. When $\overline{\text{CE}}$ = 0V and CE = 5V, the WR line is enabled. |
| 24 | 27 | CE | Chip Enable. When $\overline{\text{CE}}$ = 0V and CE = 5V, the WR line is enabled. |
| 25, 27, 29, 31, 33, 35, 37, 39 | 28, 30, 32, 35, 37, 39, 41, 43 | OUT7-OUT0 | Output Buffers 7-0 (Note 1) |
| 28, 30, 32 | 31, 33, 36 | AGND | Analog Ground must be at 0.0V since the gain resistors of the buffers are tied to these 3 pins. |
| 36 | 40 | D3 | Parallel Data Bit D3 when SER/ $\overline{\text{PAR}}$ = 0V. When D3 = 0V, D0-D2 specifies the input channel to be connected to buffer. When D3 = 5V, then D0-D2 specify control codes. D3 is not used when SER/ $\overline{\text{PAR}}$ = 5V. |
| 38 | 42 | D2 | Parallel Data Bit D2 when SER/ $\overline{\text{PAR}}$ = 0V. Not used when SER/ $\overline{\text{PAR}}$ = 5V. |

Note 1: Buffer inputs are internally grounded with a 1000 or 1001 command from the D3-D0 lines. AGND must be at 0.0V since the gain setting resistors of the buffers are internally tied to AGND.

8 x 8 Video Crosspoint Switch

MAX456

Detailed Description

Output Buffers

The MAX456 video crosspoint switch consists of 64 T-switches in an 8 x 8 grid (Figure 1). The 8 matrix outputs are followed by 8 wideband buffers optimized for driving 400 Ω and 20pF loads. Each buffer has an internal active load on the output that can be readily shut off via the LOAD input (off when LOAD = 0V). The shut-off is useful when two or more MAX456 circuits are connected in parallel to create more input channels. With more input channels, only one set of buffers can be active and only one set of loads can be driven. And, when active, the buffer must have either 1) an internal load, 2) the internal load of another buffer in another MAX456, or 3) an external load.

Each MAX456 output can be disabled under logic control. When a buffer is disabled, its output enters a high-impedance state. In multichip parallel applications, the disable function prevents inactive outputs from loading lines driven by other devices. Disabling the inactive buffers reduces power consumption.

The MAX456 outputs connect easily to MAX470 quad, gain-of-two buffers when 75 Ω loads must be driven.

Power-On RESET

The MAX456 has an internal power-on reset (POR) circuit that remains low for 5 μ s when power is applied. POR also remains low if the total supply voltage is less than 4V. **The POR disables all buffer outputs at power-up**, but the switch matrix is not preset to any initial condition. The desired switch state should be programmed before the buffer outputs are enabled.

Digital Interface

The desired switch state can be loaded in a 7-bit parallel-interface mode or 32-bit serial-interface mode (see Table 3 and Figures 4-6). All action associated with the WR line occurs on its rising edge. The same is true for the LATCH line if EDGE/LEVEL is high. Otherwise, the second-rank registers update while LATCH is low (when EDGE/LEVEL is low). WR is logically ANDed with CE and $\overline{\text{CE}}$ to allow active-high or active-low chip enable.

7-Bit Parallel Mode

In the parallel-interface mode, the 7 data bits A2-A0 and D3-D0 specify an output channel (A2-A0) and the input channel to which it connects (D3-D0). The data is loaded on the rising edge of WR. The 8 input channels are selected by 0000 through 0111 (D3-D0). The remaining 8 codes (1000-1111) control other MAX456 functions, as listed in Table 1.

32-Bit Serial-Interface Mode

In serial mode (SER/PAR = high), all first-rank registers are loaded with data, making it unnecessary to specify an output address (A2, A1, A0). The input data format is D3-D0, starting with OUT0 and ending with OUT7 for 32 total bits. Only codes 0000 through 1010 are valid. Code 1010 disables a buffer, while code 1001 enables it. After data is shifted into the 32-bit first-rank register, it is transferred to the second rank by the LATCH line (see Table 2).

8 x 8 Video Crosspoint Switch

Table 1. Parallel-Interface Mode Functions

| A2-A0 | D3-D0 | FUNCTION |
|-------------------------------------|---------------|--|
| Selects Output Buffer, OUT0 to OUT7 | 0000 to 0111 | Connect the buffer selected by A2-A0 to the input channel selected by D3-D0. |
| | 1000 | Connect the buffer selected by A2-A0 to DGND. Note, if the buffer output is on, its output is its offset voltage. |
| | 1011 | Shut off the buffer selected by A2-A0, and retain 2nd-rank contents. |
| | 1100 | Turn on the buffer selected by A2-A0, or restore the previously connected channel. |
| | 1101 | Turn off all buffers, or leave 2nd-rank registers unchanged. |
| | 1110 | Turn on all buffers, or restore the previously connected channels. |
| | 1111 | Send a pulse to the 2nd-rank registers to load them with the contents of the 1st-rank registers. When latch is held high, this "software-LATCH" command performs the same function as pulsing LATCH low. |
| | 1001 and 1010 | Do not use these codes in the parallel-interface mode. These codes are for the serial-interface mode only. |

Table 2. Serial-Interface Mode Functions

| D3-D0 | FUNCTION |
|--------------|--|
| 0000 to 0111 | Connect the selected buffer to the input channel selected by D3-D0. |
| 1000 | Connect the input of the selected buffer to GND. Note, if the buffer output remains on, its input is its offset voltage. |
| 1001 | Turn on the selected buffer and connect its input to GND. Use this code to turn on buffers after power is applied. The default power-up state is all buffers disabled. |
| 1010 | Shut off the selected buffer at the specified channel, and erase data stored in the 2nd rank of registers. The 2nd rank now holds the command word 1010. |
| 1011 to 1111 | Do not use these codes in the serial-interface mode. They inhibit the latching of the 2nd-rank registers, which prevents proper data loading. |

8 x 8 Video Crosspoint Switch

MAX456

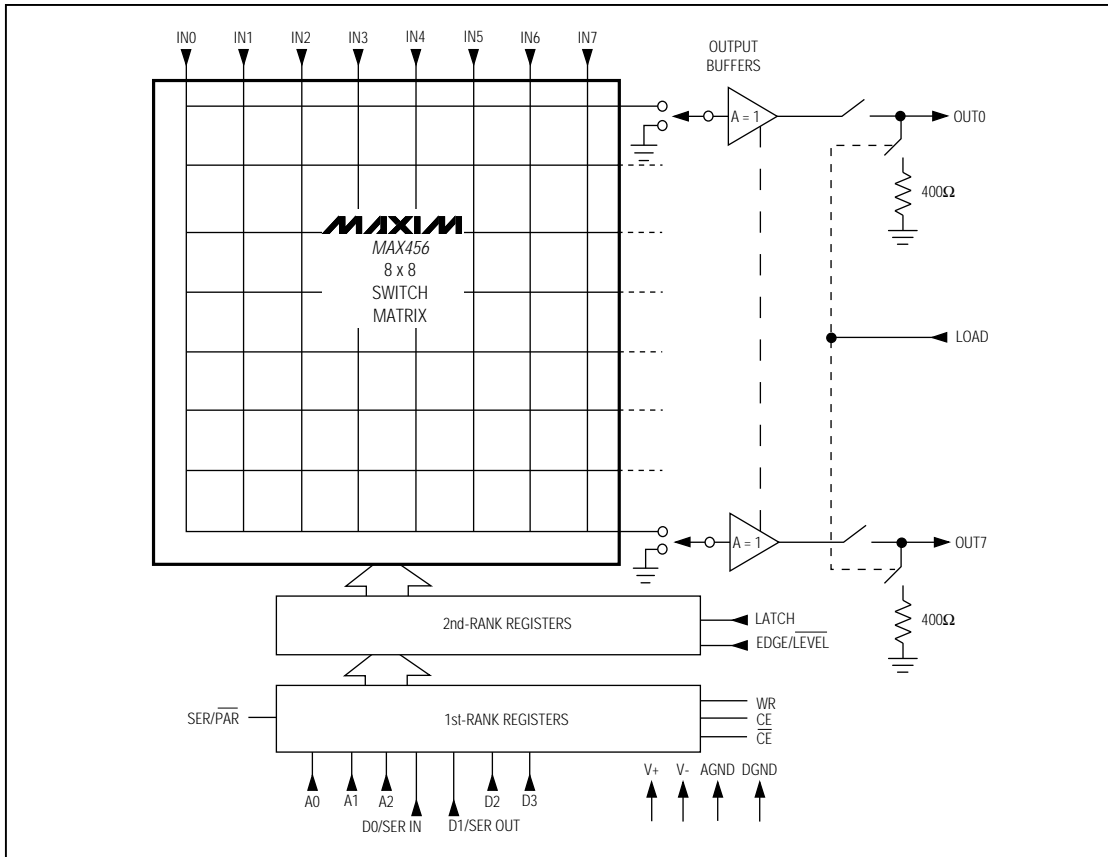


Figure 1. MAX456 Functional Diagram

Table 3. Input/Output Line Configurations

| SERIAL/ PARALLEL | D3 | D2 | D1 | D0 | A2-A0 | COMMENT |
|---------------------|----|----------------|----------------|----------------|-----------------------|--------------------------------------|
| H | X | X | Serial Output | Serial Input | X | 32-Bit Serial Mode |
| L | H | Parallel Input | Parallel Input | Parallel Input | Output Buffer Address | Parallel Mode, D0-D2 = Control Code |
| L | L | Parallel Input | Parallel Input | Parallel Input | Output Buffer Address | Parallel Mode, D0-D2 = Input Address |

Note : X = Don't Care, H = 5V, L = 0V

8 x 8 Video Crosspoint Switch

Typical Application

Figure 2 shows a typical application of the MAX456 with MAX470 quad, gain-of-two buffers at the outputs to drive 75Ω loads. This application shows the MAX456 digital-switch control interface set up in the 7-bit parallel mode. The MAX456 uses 7 data lines and 2 control lines (WR and LATCH). Two additional lines may be needed to control CE and LOAD when using multiple MAX456s.

The input/output information is presented to the chip at A2-A0 and D3-D0 by a parallel printer port. The data is stored in the 1st-rank registers on the rising edge of WR. When the LATCH line goes high, the switch configuration is loaded into the 2nd-rank registers, and all 8 outputs enter the new configuration at the same time.

Each 7-bit word updates only one output buffer at a time. If several buffers are to be updated, the data is individually loaded into the 1st-rank registers. Then, a single LATCH pulse is used to reconfigure all channels simultaneously.

The short Basic program in Figure 3 loads programming data into the MAX456 from any IBM PC or compatible. It uses the computer's "LPT1" output to interface to the circuit, then automatically finds the address for LPT1 and displays a table of valid input values to be used. The program does not keep track of previous commands, but it does display the last data sent to LPT1, which is written and latched with each transmission.

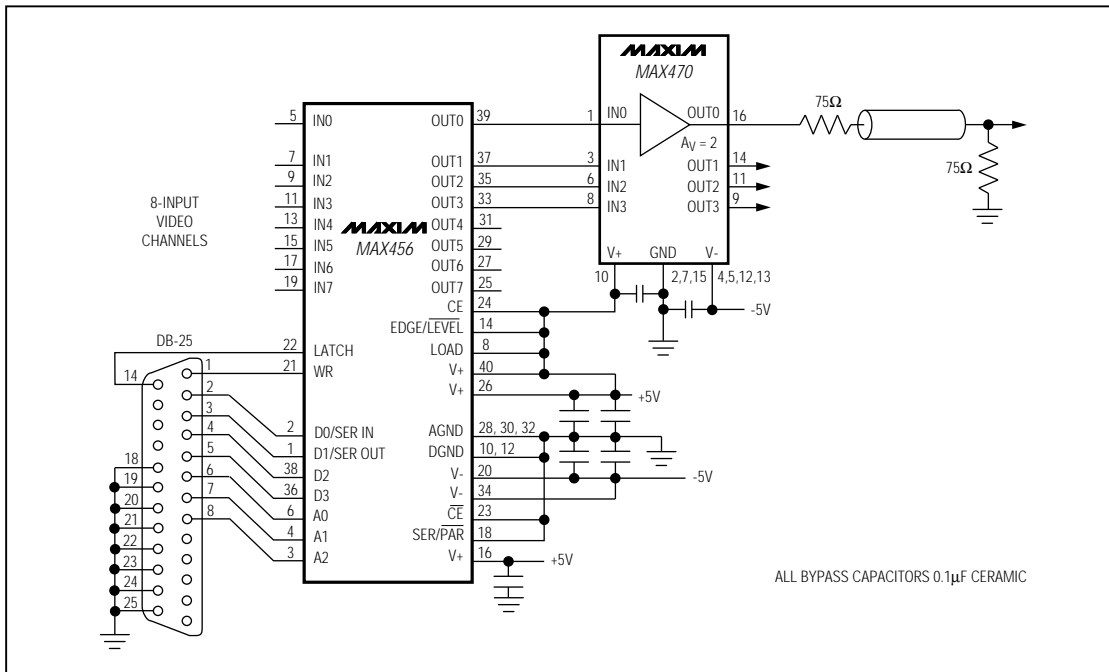


Figure 2. Typical Application Circuit

8 x 8 Video Crosspoint Switch

MAX456

```

10 REM MAX456st rev. 4/26/90 : CLS
20 DIM VALU(5,5): COL=17 : RO=5
30 DEF SEG=&H0 : ADDRESS=(PEEK(&H409)*256)+(PEEK(&H408))
40 LOCATE RO-4,COL-2 : PRINT"MAX456 8 X 8 CROSSPOINT SWITCH "
50 LOCATE RO+8,COL-12 : PRINT " Input and control codes:"
60 LOCATE RO+10,COL-16 : PRINT "0 to 7 = Valid channel and buffer input values"
70 LOCATE RO+11,COL-12 : PRINT " 8 = Specify Buffer input to connect to ground"
80 LOCATE RO+12,COL-12 : PRINT "11 = Shut off specified Buffer output"
90 LOCATE RO+13,COL-12 : PRINT "12 = Turn on specified Buffer output"
100 LOCATE RO+14,COL-12 : PRINT "13 = Shut off all Buffer outputs"
110 LOCATE RO+15,COL-12 : PRINT "14 = Turn on all Buffer outputs"
120 LOCATE RO+16,COL-12 : PRINT " E = End Program"
130 LOCATE RO+0,COL+21 : PRINT " "
140 LOCATE RO-1,COL+5 : PRINT "Input Channel or "
150 LOCATE RO+0,COL+5 : INPUT "Control Code ? ",CH$ : REM D0-D3
160 CH=VAL(RIGHT$(CH$,2)) : IF CH<0 OR CH>15 OR CH=9 OR CH=10 THEN 130
170 IF RIGHT$(CH$,1)="E" OR RIGHT$(CH$,1)="e" THEN END
180 LOCATE RO+1,COL+5 : INPUT "Buffer Output ? ",AM$ : REM A0-A2
190 LOCATE RO+1,COL+21 : PRINT " "
200 AM=VAL(RIGHT$(AM$,1)) : IF AM<0 OR AM>7 THEN 180
210 LOCATE RO+3,COL+5 : PRINT "OUTPUT VALUES"
220 LOCATE RO+4,COL+5 : PRINT "DATA=";CH :LOCATE RO+4,COL+15 :PRINT" BUF=";AM
230 OUT ADDRESS,(AM*16)+CH: REM DATA OUT
240 OUT ADDRESS+2,1 : REM Write low DB25-1
250 OUT ADDRESS+2,2 : REM Latch low DB25-14 and WR hi DB25-1
260 OUT ADDRESS+2,0 : REM take Latch hi
270 GOTO 130
    
```

Figure 3. BASIC Program for Loading Data into the MAX456 from a PC Using Figure 2's Circuit

Timing Diagrams

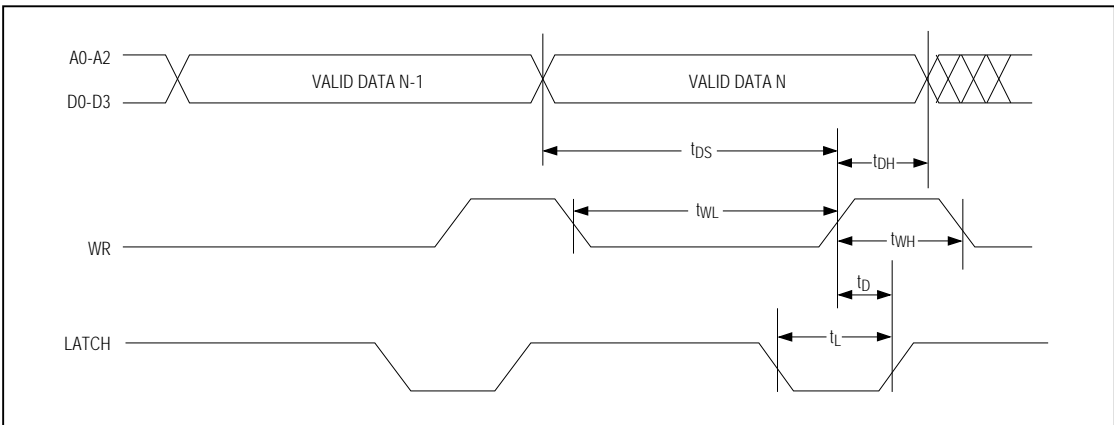


Figure 4. Write Timing for Serial- and Parallel-Interface Modes

8 x 8 Video Crosspoint Switch

Timing Diagrams (continued)

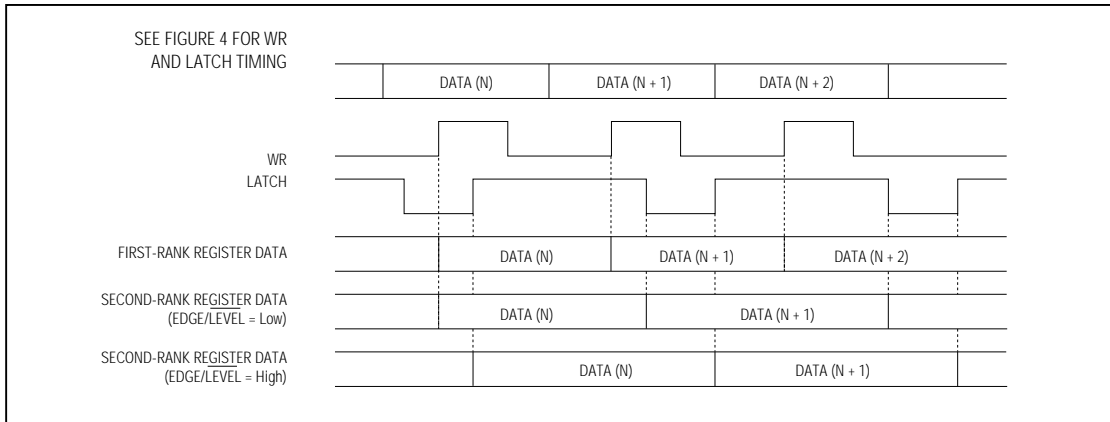


Figure 5. Parallel-Interface Mode Format ($SER/\overline{PAR} = Low$)

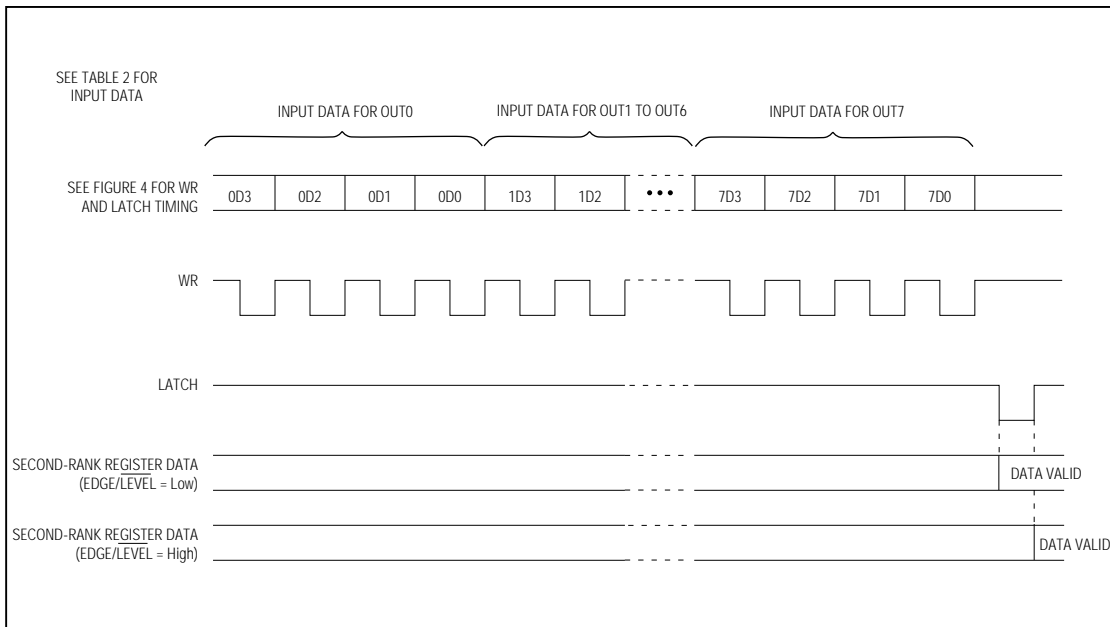
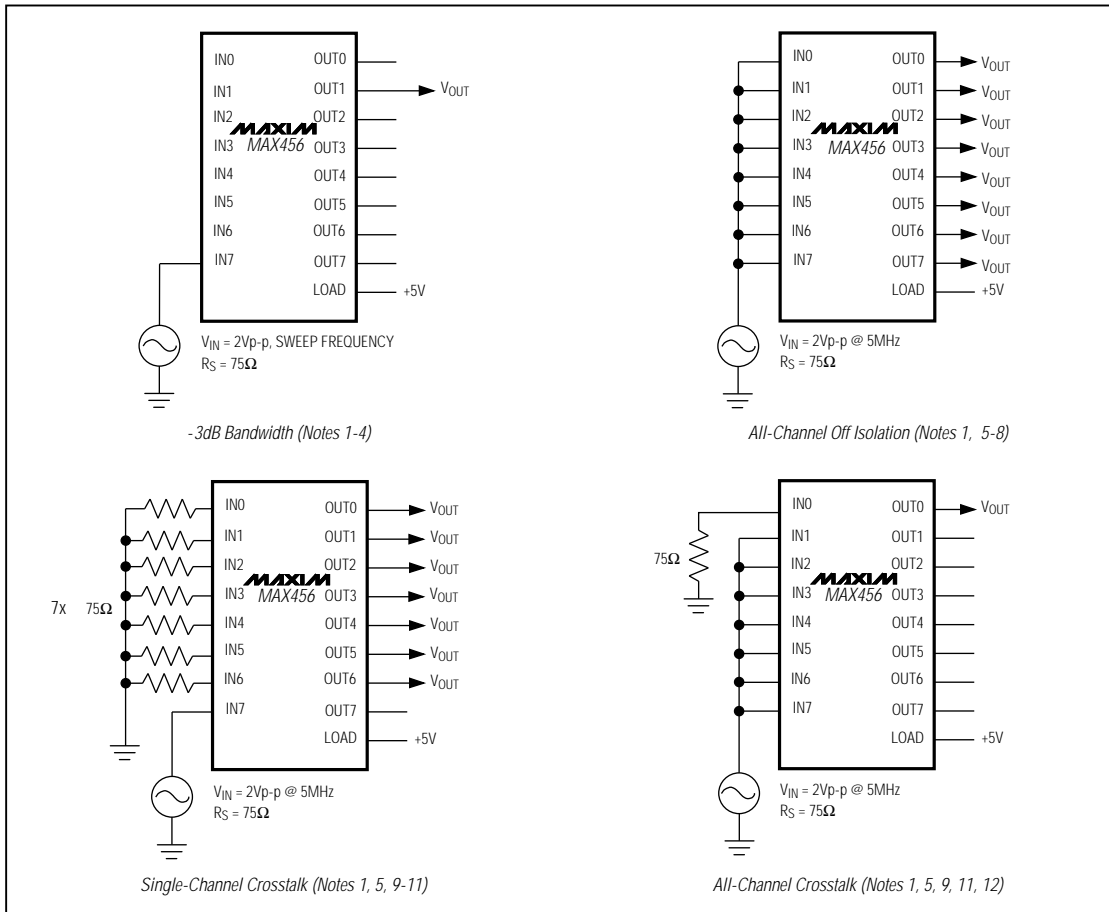


Figure 6. 32-Bit Serial-Mode Interface Format ($SER/\overline{PAR} = High$)

8 x 8 Video Crosspoint Switch

Dynamic Test Circuits

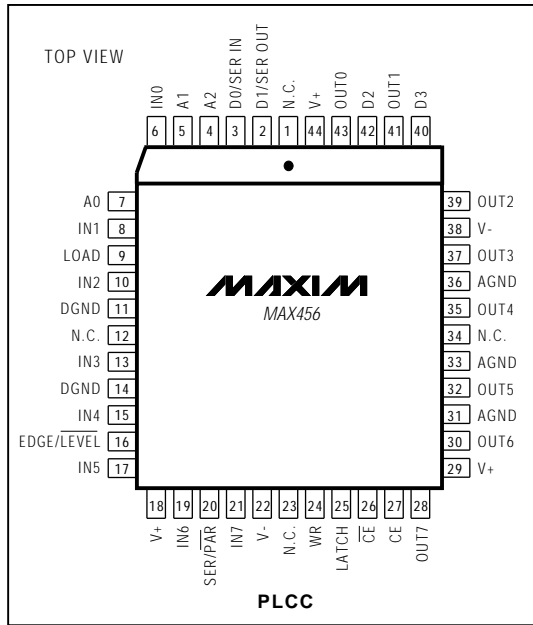
MAX456



- Note 1:** Connect LOAD (pin 8) to +5V (internal 400Ω loads on at all outputs).
- Note 2:** Program any one input to connect to any one output (see Table 1 or 2 for programming codes).
- Note 3:** Turn on buffer at the selected output (see Table 1 or 2).
- Note 4:** Drive the selected input with V_{IN} , and measure V_{OUT} at the -3dB frequency at the selected output.
- Note 5:** Program each numbered input to connect to the same numbered output (IN0 to OUT0, IN1 to OUT1, etc.). See Table 1 or 2 for programming codes.
- Note 6:** Turn off all output buffers (see Table 1 or 2).
- Note 7:** Drive all inputs with V_{IN} and measure V_{OUT} at any output.
- Note 8:** Isolation (in dB) = $20\log_{10}(V_{OUT}/V_{IN})$.
- Note 9:** Turn on all output buffers (see Table 1 or 2).
- Note 10:** Drive any one input with V_{IN} and measure V_{OUT} at any undriven output.
- Note 11:** Crosstalk (in dB) = $20\log_{10}(V_{OUT}/V_{IN})$.
- Note 12:** Drive all but one input with V_{IN} and measure V_{OUT} at the undriven output.

8 x 8 Video Crosspoint Switch

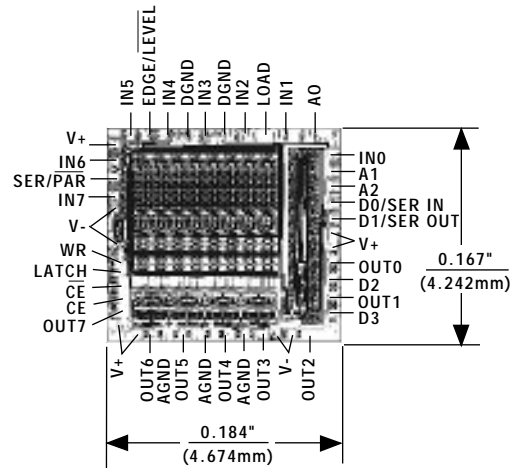
Pin Configurations (continued)



Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE |
|-----------|----------------|----------------|
| MAX456EPL | -40°C to +85°C | 40 Plastic DIP |
| MAX456EOH | -40°C to +85°C | 44 PLCC |
| MAX456EJL | -40°C to +85°C | 40 CERDIP |

Chip Topography



TRANSISTOR COUNT: 3820;
SUBSTRATE CONNECTED TO V+.

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